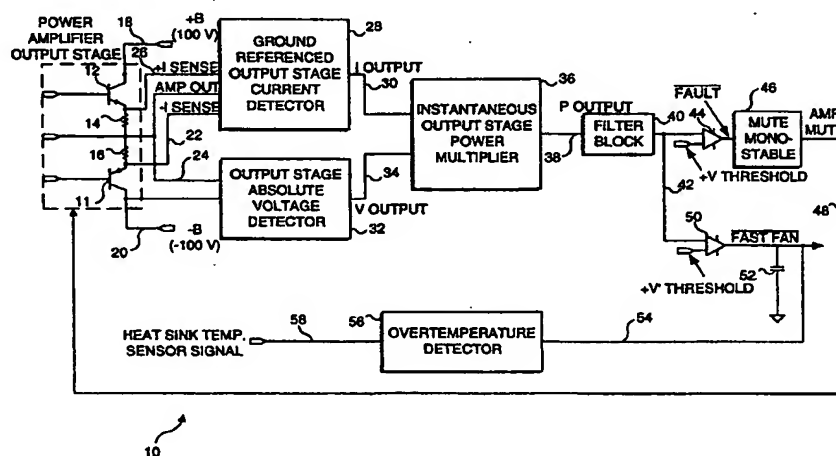




## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification <sup>6</sup> : <b>H02H 3/18</b>	<b>A1</b>	(11) International Publication Number: <b>WO 00/19572</b> (43) International Publication Date: 6 April 2000 (06.04.00)
(21) International Application Number: PCT/US99/18902 (22) International Filing Date: 20 August 1999 (20.08.99) (30) Priority Data: 09/164,199          30 September 1998 (30.09.98)    US (71) Applicant: MACKIE DESIGNS INC. [US/US]; 16220 Wood- invillie-Redmond Road N.E., Woodinville, WA 98072 (US). (72) Inventors: JONES, Cameron; 1567 Sky Terrace S.E., Salem, OR 97306 (US). PERKINS, Calvin, C.; 12354 N.W. Kearney Street, Portland, OR 97229 (US). (74) Agent: ANDERSON, Ronald, M.; Law Offices of Ronald M. Anderson, Suite 507, 600 - 108th Avenue, N.E., Bellevue, WA 98004 (US).		(81) Designated States: BR, CA, CN, JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  <b>Published</b> <i>With international search report.</i>

(54) Title: MONITORING OUTPUT POWER TO PROTECT A POWER AMPLIFIER



## (57) Abstract

A protection circuit (10) for a power amplifier mutes the amplifier if the average power dissipated in the amplifier output stage exceeds a predetermined limit. A ground referenced current detector (28) monitors the current through the amplifier output stage, producing a current signal (30) that is directly proportional to this output current. Similarly, an absolute voltage detector (32) monitors the voltage across the output stage, producing a voltage signal (34) that is directly proportional thereto. The current signal and voltage signal are input to a multiplier (36), which multiplies them to determine their product, producing a power signal (38), which is directly proportional to the power dissipated in the output stage. This power signal is filtered to represent the average power dissipation in the output stage. The filtered signal (42) is then compared (44) to a threshold signal representing a predefined power dissipation limit. A monostable multi-vibrator (46) periodically mutes the amplifier so long as the power dissipated exceeds the predefined limit. In addition to being used for muting the power amplifier, the filtered power output signal (42) is employed for controlling the speed of a cooling fan.

**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakhstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

## **MONITORING OUTPUT POWER TO PROTECT A POWER AMPLIFIER**

### **Field of the Invention**

This invention generally relates to a protection circuit for a power  
5 amplifier, and more specifically, to a protection circuit for a power amplifier that  
is responsive to the output power of the amplifier.

### **Background of the Invention**

The manner in which a power amplifier is used represents a potential weak  
point in its design. Misuse of a power amplifier can occur in a variety of ways.  
10 For example, a user might connect more speakers to an amplifier than is  
recommended, so that the effective impedance of the load is much less than a  
recommended minimum for the amplifier. Or, either the output terminals or  
speaker wires can be accidentally shorted, creating a path for excessive current  
draw from the output stage of an amplifier. These are but two examples of the  
15 many damaging operating conditions to which an amplifier might be subjected.  
To improve the likelihood that a power amplifier will survive such mistreatment  
by a user, various protection mechanisms have been employed in the prior art.

Most prior art power amplifier protection schemes center around  
protecting the output stage, since the power amplifier transistors used in this  
20 portion of an amplifier are often relatively expensive to replace if damaged.  
While such protection methods may protect the output stage from failure, this type  
of protection often adversely affects an amplifier's perceived sound quality and  
performance. Conventional limiting circuits that are used for output stage  
protection typically employ current and/or voltage limits that must be set  
25 sufficiently low to protect the output stage. In conventional current/voltage  
limiting, which is used when driving typical reactive speaker loads, the output  
stage is momentarily turned off on a cycle by cycle basis (i.e., during each cycle  
of the output signal) to achieve the required protection. This cyclic interruption  
occurring in the sound field of the speaker produces very audible (and readily  
30 measurable) distortion. The level of distortion increases as the output stage of the

power amplifier is driven further beyond the limit at which the protection scheme first becomes active and begins to cycle the output stage off.

In response to market demand, power amplifiers are being designed with ever greater power output levels. Accordingly, it is becoming increasingly cost effective to employ elaborate protection schemes to prevent damage to the rather expensive output stages of these amplifiers. The added cost of such protection is more than offset by the substantially higher cost of replacing the output transistors and other output circuit components that would be required if a power amplifier without adequate protection is damaged and the reduction in field repair costs resulting from increased product reliability.

However, it would clearly be preferable to employ a protection circuit that is economical to minimize the overall product cost of a power amplifier. An appropriate protection circuit should increase power amplifier reliability, without causing any degradation of sound quality like that caused by conventional output stage protection circuits. While such a protection circuit may employ voltage/current limiting, the sensitivity of the protection circuit should be minimized to facilitate the maximum transient safe operating area (SOA) available from the output stage of the amplifier. Highly reactive loading should not cause the protection circuit to generate distortion. Ideally, a protection circuit should determine the heating effect of the load on the output stage, and mute the power amplifier for a period that is much longer than a cycle of the drive signal, but only when this heating effect is excessive. By muting the amplifier for several seconds when the rated limit is exceeded, a clear audible indication can be provided that the rated power limit of the amplifier is being exceeded, without introducing distortion in the output signal before the protection is actually required. Currently, there does not appear to be any prior art protection circuit that implements all of the above-described functions.

#### Summary of the Invention

In accord with the present invention, a protection circuit for an amplifier having at least one channel is defined. The protection circuit includes a current detector that produces a current signal, which is directly proportional to the current being pulled through the output stage. A voltage detector is included and produces a voltage signal that is directly proportional to a voltage across the output stage. Coupled to the current detector and to the voltage detector to receive the current signal and the voltage signal is a power stage dissipation monitor, which produces a power signal that is directly proportional to the instantaneous output stage dissipation (power), by multiplying the current signal

by the voltage signal. A multiplier circuit is used in a preferred form of the invention to determine the product of the current signal and the voltage signal. A muting circuit is coupled to the power stage dissipation monitor and mutes the one or more channels of the amplifier for a predefined interval of time if the power  
5 signal exceeds a predefined level.

Also preferably included in the protection circuit is a filter that couples the muting circuit to the power stage dissipation monitor. The filter averages the power signal, producing an average power signal. The filter passband is below the amplifier's intended band of usage, such that the output of the filter is  
10 representative of the average power dissipation in the output stage.

The muting circuit includes a comparator that compares the average power signal with a threshold signal. This threshold signal is preferably set to a predefined level coinciding with the point at which safe operation of the output stage cannot be readily guaranteed. Furthermore, the muting circuit produces a  
15 muting signal that periodically mutes the amplifier for a first interval of time, and then enables the amplifier to produce the drive signal for a second interval of time. Thus, the drive signal periodically cycles between a muted state and an enabled state, until the muting circuit determines that the average power signal is less than the predefined level. The first interval of time is preferably substantially  
20 longer than the second interval of time so that an average power dissipation by the amplifier cycling between the muted state and the enabled state is substantially less than it would be if the amplifier were not periodically muted.

The muting circuit produces a signal that preferably mutes the amplifier to interrupt the power delivered to the load, thus reducing the output stage power  
25 demand to zero. The amplifier is muted either by activating an output relay that disconnects the load from the amplifier, and/or by shunting the input signal applied to the amplifier to eliminate the drive signal, and/or by interrupting a bias applied to one or more voltage amplifying stages of the amplifier that effectively "turns off" the amplifier.

30 In one preferred embodiment, the amplifier also includes a cooling fan, and a temperature detector that monitors a temperature of the output stage, producing a temperature signal. A fan control circuit is coupled to the power stage dissipation monitor and the temperature detector. This fan control circuit produces a fan speed control signal that determines a speed of the cooling fan as a  
35 function of the temperature signal and the power signal.

Another aspect of the present invention is a method for protecting an amplifier that includes at least one channel, from damage due to excessive power

supplied to a load connected to the amplifier. The steps of the method are generally consistent with the functions implemented by the elements of the protection circuit discussed above.

#### **Brief Description of the Drawing Figures**

5       The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

10       FIGURE 1 is a schematic functional block diagram of the protection circuit implemented in a preferred embodiment of the present invention;

      FIGURE 2 is a schematic diagram showing details of an output stage current detector employed in a preferred embodiment of the present invention;

15       FIGURE 3 is a schematic diagram showing details of an output stage absolute voltage detector used in a preferred embodiment of the present invention; and

      FIGURE 4 is a graph illustrating an exemplary periodic waveform for the output signal from one channel of a power amplifier caused by the protection circuit during a fault condition.

#### **Description of the Preferred Embodiment**

20       A preferred embodiment of a protection circuit 10 representing the present invention is illustrated in FIGURE 1. It should be noted that protection circuit 10 is usable in a power amplifier having a single channel, or alternatively, may be applied in amplifiers having two or more channels. Since each channel of a multi-channel amplifier will likely have different input signals and may have different  
25       loads coupled to them, it may be preferable to independently apply the present invention for separately protecting each channel of the amplifier. Alternatively, it may be desirable to protect all channels of the amplifier if any one of the channels is overdriven. The manner in which the protection is applied will depend upon the type of amplifier, its usage, and its design.

30       Virtually all power amplifiers include an output stage in which relatively expensive power transistors are employed for amplifying the current supplied to drive speakers or other type of load. Details of the power amplifier output stage are not illustrated in FIGURE 1. Instead, only power transistors 11 and 12 are shown to illustrate how a preferred embodiment senses current and voltage of the  
35       drive signal "AMP-OUT," which is provided by the power amplifier from its output stage for a single channel of the power amplifier. The other channel of this power amplifier has an identical protection circuit.

In the illustrated preferred embodiment of FIGURE 1, power transistor 11 is a PNP type, and power transistor 12 is an NPN type. The emitters of the two power transistors are coupled together through resistors 14 and 16. The collector of the NPN power transistor is coupled to a positive voltage rail (+B, which is 100 volts in this example) through a lead 18, while the collector of the PNP power transistor is connected to the negative voltage rail (-B, which is -100 volts in this example) through a lead 20. The amplifier output signal is provided on the common connection between resistors 14 and 16 as an input to a ground referenced output stage current detector 28. Also applied as inputs to the current detector are a positive current sense signal, "+I SENSE," on a line 26 connected to the emitter of NPN power transistor 12, and a negative current sense signal, "-I SENSE," which is obtained from the emitter of the PNP power transistor. While it might appear simpler to obtain a ground referenced voltage proportional to output stage current by inserting a shunt resistor in series with the return output terminal of the amplifier and ground, this option was not possible in power amplifiers in which the present invention will initially be used because it includes two channels that can optionally be bridged together to provide a single monophonic channel with twice the power of the two channels. In this bridge mode of operation, current is not returned to the speaker ground connector output terminals of the power amplifier. Accordingly, in the preferred embodiment illustrated in FIGURE 1, the voltage drop across resistors 14 and 16 for current flowing through the output power transistors provides the corresponding positive and negative current sense signals that are input to ground referenced output stage current detector 28.

Details of the ground referenced output stage current detector are shown in FIGURE 2. As indicated therein, the positive current sense signal is input through a resistor 60 to the non-inverting input of an operational amplifier (opamp) 68. The inverting input of the opamp is connected to receive the negative current sense signal that is applied through a resistor 64. A resistor 62 and a capacitor 66 are coupled between the non-inverting input of opamp 68 and the amplifier output signal (AMP-OUT). Feedback around opamp 68 includes a resistor 70 in parallel with a capacitor 72. This circuit is a simple balanced input amplifier having equal inverting and non-inverting gains (so long as the ratio of resistors 60 and 62 is equal to that of resistors 64 and 70). Capacitor 72 is required to improve the high frequency stability for the particular opamp used in this embodiment, and capacitor 66 is employed to keep the inverting and non-inverting gains equal at high frequencies. Since the AMP-OUT/+I SENSE signal is positive and the

AMP-OUT/-I SENSE signal is negative, this stage also acts as a full wave positive rectifier referred to the AMP-OUT line.

The output of opamp 68 is applied to the non-inverting input of an opamp 74, while its inverting input is connected to an emitter of an NPN transistor 82. The anode of a diode 76 is coupled to the inverting input of opamp 74 and is the feedback path for the opamp. The output of opamp 74 is also connected to a resistor 78, the other end of which is connected to the anode of a diode 80. The cathode of diode 80 is connected to the base of NPN transistor 82, and the base of this transistor is also connected to the amplifier output signal through a resistor 84. A resistor 86 connects the amplifier output signal back to the emitter of this transistor. Opamp 74 and its associated components form a voltage-to-current converter. When a voltage that is greater than AMP-OUT is present at the non-inverting input of opamp 74, the inverting input matches this voltage due to the feedback provided by resistor 78, diode 80, NPN transistor 82, and resistor 86. The current through resistor 86 is directly proportional to the voltage at the inverting input to opamp 74. This proportional current is available as an output at the collector of NPN transistor 82. Resistor 84 provides a local return path for NPN transistor 82. Diodes 76 and 80 minimize any negative going voltage swing, ensuring the fastest recovery from an erroneous input signal to the non-inverting input of opamp 74.

The collector of NPN transistor 82 is connected to the cathode of a diode 94, and the anode of the diode is connected through a resistor 92 to the +110V +B source. Coupled in parallel with series-connected resistor 92 and diode 94 is a capacitor 96. The cathode of diode 94 and one side of capacitor 96 are coupled to the base of an PNP transistor 100. Its emitter is connected through a resistor 98 to the +110V +B rail, and its collector is connected to an output current adjuster circuit 104 and through a resistor 102 to ground. Output current adjuster circuit 104 is adjusted so that a voltage of the current output signal, "I OUTPUT," that it produces on a line 30 is defined by:

$$I_{\text{OUTPUT}}(V) = \frac{|\text{output stage current}|}{10}$$

PNP transistor 100 and the components associated with it are employed as a simple current mirror that eventually allows the signal to change its reference from AMP-OUT to ground. The current through resistor 86 will be equal to the current through resistor 92, and the voltage drop across resistor 92 will be equal to the voltage drop across resistor 98, since diode 94 matches the  $V_{be}$  drop across



PNP transistor 100. All of this circuitry is biased from a supply voltage that is greater than the peak output level available at AMP-OUT. In the preferred embodiment, AMP-OUT can be as great as +100V but never as great as the +110V supply. The current through resistor 98 is equal to the current at the collector of PNP transistor 100, and this current in turn modulates the voltage drop across resistor 102 and output current adjuster 104, which are referred to ground.

It is important to select NPN transistor 82 to be a type having a very low  $C_{ob}$ . The junction capacitance of this transistor and of capacitor 96 form a high frequency capacitive divider. This divider prevents high slewing negative going signals (60V/uS in the preferred embodiment) from improperly causing PNP transistor 100 to conduct.

In addition to its connection to ground referenced output stage current detector 28 for providing the current output signal, "I OUTPUT," the amplifier output signal line is connected through a resistor 88 to a transient fault detector (not shown). The input signals to the transient fault detector are applied on a line 108 and on line 30; a capacitor 90 between line 108 and ground allows for precise time alignment of these two signals for use in the transient fault detector. Details of the transient fault detector are not disclosed herein, since it is not part of the present invention. However, the transient fault detector provides protection for the output stage against relatively short term transients of very high magnitude. In the preferred embodiment, the transient fault detector mutes the output stage if the output stage power exceeds 3000 watts for more than 10 milliseconds.

Referring back to FIGURE 1, it will be apparent that the AMP-OUT signal on line 24 and the -B rail voltage signal on line 20 are also input to an output stage absolute voltage detector 32. Details of the voltage detector as used in a preferred embodiment are illustrated in FIGURE 3. With reference to FIGURE 3, the amplifier output signal is applied both through a resistor 110 and a resistor 112, while the -B rail voltage is input through a resistor 114. Resistors 112 and 114 are both connected to the inverting input of an opamp 124 and to one side of a resistor 115. The other side of resistor 115 is connected the junction between the cathode of a diode 120 and a resistor 122. Series-connected diode 120 and resistor 122 comprises part of a feedback loop for an operational amplifier 116. The other part of the feedback loop is a diode 118 having its anode connected to the inverting input of opamp 116 (along with the junction of resistors 110 and 122). The cathode of diode 118 and the anode of diode 120 are

both connected to the output terminal of opamp 116. Its non-inverting input is connected to ground, as is the non-inverting input of opamp 124.

A resistor 126 comprises a feedback loop between the output of opamp 124 and its inverting input, thereby controlling the gain of a voltage output signal, "V OUTPUT," which provided on a line 34. The values of this signal, which is directly proportional to the instantaneous voltage across each half (positive and negative) portion of the output stage output signal waveform is defined by:

$$V OUTPUT(V) = \frac{-(-B) - |AMP OUT|}{10}$$

Op-amp 116, with it's associated current steering parts (diodes 118 and 120, and resistor 122), acts as a full wave rectifier when it's output is current summed via resistors 112 and 115 at the virtual ground formed by ground referenced op-amp 124. Resistor 114 also adds current to this summing junction such that when AMP-OUT is centered, the voltage signal output on line 34 is most positive. As AMP-OUT approaches either the + or -100 V rail, the voltage on line 34 goes to zero.

Again referring back to FIGURE 1, the current output signal I OUTPUT on line 30 and the voltage output signal V OUTPUT on line 34 are applied as inputs to an instantaneous output stage power multiplier 36. The power multiplier includes an integrated circuit multiplier chip that determines the product of these two signals. The power multiplier multiplies the two signals together, producing an output stage power/dissipation signal, "P OUTPUT," on a line 38. This power output signal is thus equal to the product of the voltage output and current output signals and is defined in this preferred embodiment by:

$$POUTPUT(V) = \frac{|outputstagecurrent| \times |voltageacrosseachhalf of outputstage|}{200} = 200W/V$$

Line 38 is input to a filter block 40, which includes a simple single order low-pass filter comprising a capacitor and resistor (not separately shown) for filtering out frequencies in the amplifier passband from the power output signal, P OUTPUT. The filtered power output signal produced by this low pass filter is directly proportional to the average dissipation in the output stage. The half power point of the filter used in filter block 40 is 1 Hz. The filtered power output signal produced by filter block 40 is conveyed on a line 42 to a comparator 44, which compares it to a +V threshold voltage corresponding to a predefined limit

of the output power level. If the filtered power output signal exceeds the +V threshold limit, which corresponds to an output power of approximately 1000 watts in a preferred embodiment of the invention, the output signal from comparator 44 goes to a low voltage state indicative of a fault condition, represented by "FAULT." This signal is input to a mute monostable multi-vibrator 46, which produces an amplifier muting signal, "AMP MUTE," on a line 48.

In the preferred embodiment, a mute monostable multi-vibrator 46 is designed to mute the power amplifier based upon the state of the amplifier mute signal for a period of approximately four seconds, followed by a period of 0.4 seconds in which the mute signal is turned off, enabling the power amplifier to again produce an output signal. So long as the power dissipated by the output stage of the power amplifier continues to exceed the 1000 watt threshold during this 0.4 seconds in which the output stage is again enabled, the mute monostable multi-vibrator will continue to cycle the output stage of the power amplifier off for successive intervals of approximately four seconds duration. As shown in FIGURE 4, if the amplifier output terminals are shorted, the output power of the power amplifier will have the periodic waveform illustrated in which the amplifier is energized during short pulses 140 lasting approximately 0.4 seconds, followed by periods 142 of approximately four seconds duration in which the amplifier is muted. When the short is removed from the terminal, the amplifier will be enabled, enabling it to continue to produce music in accordance with the input signal that it is supplied. In this exemplary preferred embodiment, the average power dissipation during continuous fault conditions is approximately equal to:

$$P_{avg} = \frac{1000 \text{ W} \times 0.4 \text{ sec}}{4 \text{ sec}} = 100 \text{ W}$$

Again referring back to FIGURE 1, the filtered power output signal on line 42 is also applied to a comparator 50 for comparison to a +V' threshold voltage. If the output from comparator 50 is low, the "FAST FAN" speed signal that is output to control a cooling fan (not shown) may cause the fan speed to increase. A capacitor 52 is connected between the output of comparator 50 and ground. In addition, a line 54 from an overtemperature detector 56 is connected to the output of comparator 50. Overtemperature detector 56 receives an input temperature signal from a heat sink temperature sensor (not shown) on a line 58, which indicates the temperature of power transistors 12 (or the temperature of the amplifier chassis, another component, or some other sensitive portion of the

power amplifier). Based upon the temperature determined by overtemperature detector 56, it produces an output signal on line 54. This signal on line 54 is summed with the signal from comparator 50 to control the fan speed.

5 In a preferred embodiment of the invention, the fan speed increases from a slow state when the temperature of the output stage is below 45°C, ramping to its fastest speed when the temperature is at or above 65°C. However, if the comparison of the average power signal with the +V' threshold indicates that the average power being dissipated from the power amplifier is below 150 watts, the cooling fan reverts to its slow speed.

10 In the preferred embodiment of the present invention, the amplifier mute signal produced by mute monostable multi-vibrator 46 mutes the power amplifier by actuating relays that control the current flow to the output terminals of the power amplifier and by interrupting the signal that is applied to the output stage from a voltage amplifier stage of the power amplifier. It is also contemplated that  
15 the amplifier mute signal be used in other ways to disable the output signal from the power amplifier to mute it, for example, by shunting the input signal to the amplifier and by biasing one or more stages of the power amplifier so as to effectively "turn it off." Those of ordinary skill in the art will appreciate that still other techniques can be used for employing the amplifier mute signal to  
20 periodically mute the output stage to protect against excessive average power dissipation.

Although the present invention has been described in connection with the preferred form of practicing it, those of ordinary skill in the art will understand that many modifications can be made thereto within the scope of the claims that  
25 follow. Accordingly, it is not intended that the scope of the invention in any way be limited by the above description, but instead be determined entirely by reference to the claims that follow.

The invention in which an exclusive right is claimed is defined by the following:

1. A protection circuit for an amplifier that includes at least one channel, comprising:

(a) a current detector that produces a current signal directly proportional to a magnitude of a current comprising a drive signal that is supplied by the amplifier through said at least one channel to drive a load;

(b) a voltage detector that produces a voltage signal directly proportional to a voltage of the drive signal;

(c) a power stage dissipation monitor that is coupled to the current detector and to the voltage detector to receive the current signal and the voltage signal, and which produces a power signal directly proportional to a power produced by the amplifier on said at least one channel, as a function of a product of the current signal and the voltage signal; and

(d) a muting circuit that is coupled to the power stage dissipation monitor, said muting circuit muting said at least one channel of the amplifier for a predefined interval of time if the power signal exceeds a predefined level.

2. The protection circuit of Claim 1, further comprising a filter that couples the muting circuit to the power stage dissipation monitor, and which averages the power signal by filtering higher frequency amplifier passband signals from the power signal, producing an average power signal.

3. The protection circuit of Claim 2, wherein the muting circuit includes a comparator that compares the average power signal to a threshold signal, which is indicative of a predefined safe operating level.

4. The protection circuit of Claim 1, wherein the muting circuit produces a muting signal that periodically:

(a) mutes the amplifier for a first interval of time; and

(b) enables the amplifier to produce the drive signal for a second interval of time, so that the drive signal periodically cycles between a muted state and an enabled state, until the muting circuit determines that the power signal is less than the predefined level.

5. The protection circuit of Claim 4, wherein the first interval of time is substantially longer than the second interval of time so that an average power dissipation by the amplifier cycling between the muted state and the enabled state is substantially less than it would be if the amplifier were not periodically muted.

6. The protection circuit of Claim 1, wherein the muting circuit mutes the amplifier by implementing at least one of the following:
  - (a) disabling biasing of one or more amplifier stages of the amplifier;
  - (b) shunting an input signal coupled to the amplifier to eliminate the drive signal; and
  - (c) interrupting the drive signal from the amplifier so that it no longer drives a load coupled thereto.
7. The protection circuit of Claim 6, further comprising:
  - (a) a cooling fan that cools the amplifier;
  - (b) a temperature detector that monitors a temperature of the output stage, producing a temperature signal; and
  - (c) a fan control circuit that is coupled to the power stage dissipation monitor and the temperature detector, said fan control circuit producing a fan speed control signal that determines a speed of the cooling fan as a function of the temperature signal and the power signal.
8. The protection circuit of Claim 1, wherein the power stage dissipation monitor includes a multiplier circuit that multiplies the current signal by the voltage signal, to produce the power signal.
9. A protection circuit for a power amplifier that prevents damage to an output stage of the power amplifier, comprising:
  - (a) an output stage current detector that monitors an output current from the output stage and produces a current signal directly proportional to the output current;
  - (b) an output stage absolute voltage detector that monitors an absolute voltage of the output stage and produces a voltage signal directly proportional to the absolute voltage;
  - (c) an instantaneous output stage power multiplier, coupled to the output stage current detector and the output stage absolute voltage detector, said instantaneous output stage power multiplier producing a power signal by multiplying the voltage signal by the current signal; and
  - (d) means for muting the power amplifier in response to a magnitude of the power signal exceeding a predefined power level.
10. The protection circuit of Claim 9, further comprising a low-pass filter that is connected to the instantaneous output stage power multiplier, said low-pass filter substantially averaging the power signal by filtering higher frequency amplifier passband components from the power signal, producing an average power signal that is supplied to the means for muting the power amplifier.

11. The protection circuit of Claim 9, wherein the means for muting the power amplifier comprise a monostable multi-vibrator that produces a muting signal used to periodically mute the power amplifier for a period of time substantially longer than a period of the output signal.

12. The protection circuit of Claim 9, further comprising a cooling fan controlled by a fan control circuit, said fan control circuit responding to the power signal to control a speed of the cooling fan.

13. The protection circuit of Claim 12, further comprising a temperature detector that monitors a temperature of the power amplifier to produce a temperature signal, said fan control circuit controlling a speed of the cooling fan in response to the temperature signal received from the temperature detector.

14. The protection circuit of Claim 13, wherein the fan control is also connected to the means for muting the power amplifier and controls the speed of the cooling fan in response to a signal received from the means for muting the power amplifier.

15. A method for protecting an amplifier that includes at least one channel, from damage due to excessive power supplied to a load connected to the amplifier, comprising the steps of:

(a) monitoring a magnitude of a current comprising a drive signal that is supplied by the amplifier through said at least one channel to drive the load, producing a current signal directly proportional to the magnitude of said current;

(b) monitoring a magnitude of a voltage of the drive signal, producing a voltage signal directly proportional to the magnitude of the voltage of the drive signal;

(c) producing a product directly proportional to a power produced by the amplifier on said at least one channel, by multiplying the current signal by the voltage signal; and

(d) muting said at least one channel of the amplifier for a predefined interval of time, as a function of the product of the voltage signal and the current signal.

16. The method of Claim 15, further comprising the step of averaging the product of the voltage signal and the current signal, to produce an average power signal.

17. The method of Claim 16, wherein the step of muting includes the step of comparing the average power signal to a threshold signal that is indicative of a predefined level.
18. The method of Claim 17, wherein the step of muting includes the steps of:
- (a) muting the amplifier for a first interval of time; and
  - (b) enabling the amplifier to produce the drive signal for a second interval of time, so that the drive signal cycles between a muted state and an enabled state until the average power signal is less than the threshold signal.
19. The method of Claim 18, wherein the first interval of time is substantially longer than the second interval of time so that an average power dissipation of the amplifier cycling between the muted state and the enabled state is substantially less than it would be if the amplifier were not periodically muted.
20. The method of Claim 15, wherein the step of muting includes at least one of the steps of:
- (a) disabling biasing of one or more amplifier stages of the amplifier;
  - (b) shunting an input signal coupled to the amplifier to eliminate the drive signal; and
  - (c) interrupting the drive signal from the amplifier so that it no longer drives a load coupled thereto.
21. The method of Claim 20, further comprising the steps of:
- (a) cooling the amplifier with a fan;
  - (b) monitoring a temperature of the output stage, producing a temperature signal; and
  - (c) controlling a speed of the fan as a function of the temperature signal and the power signal.



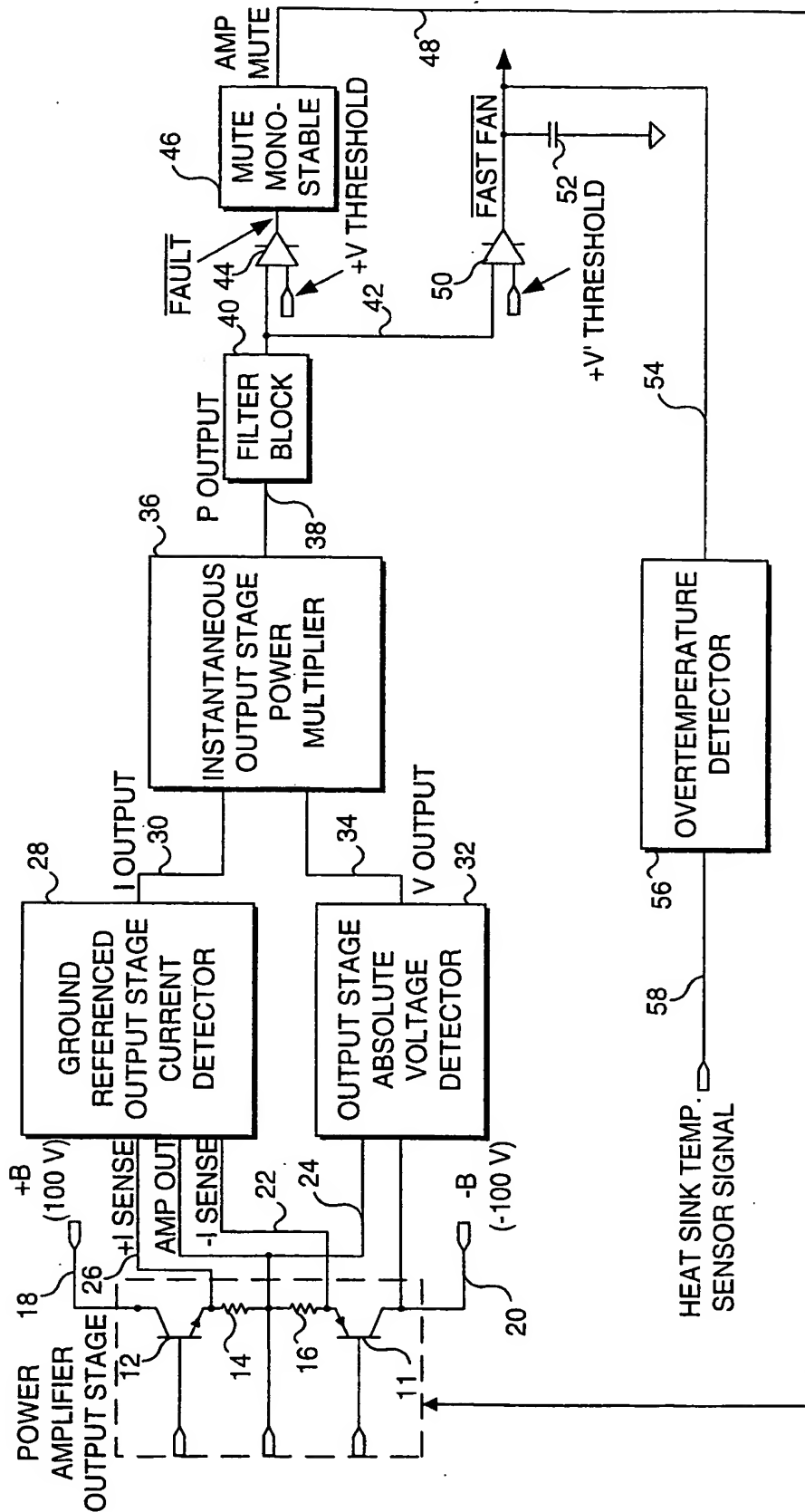
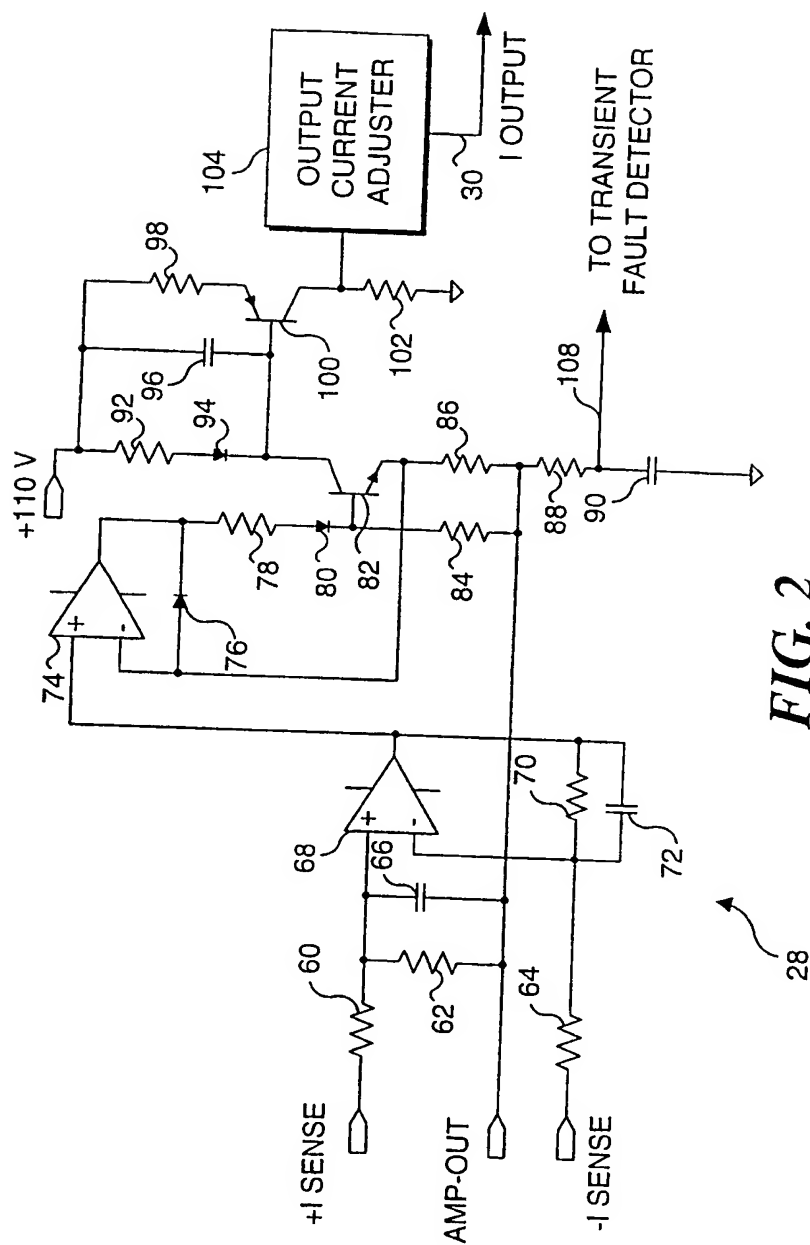
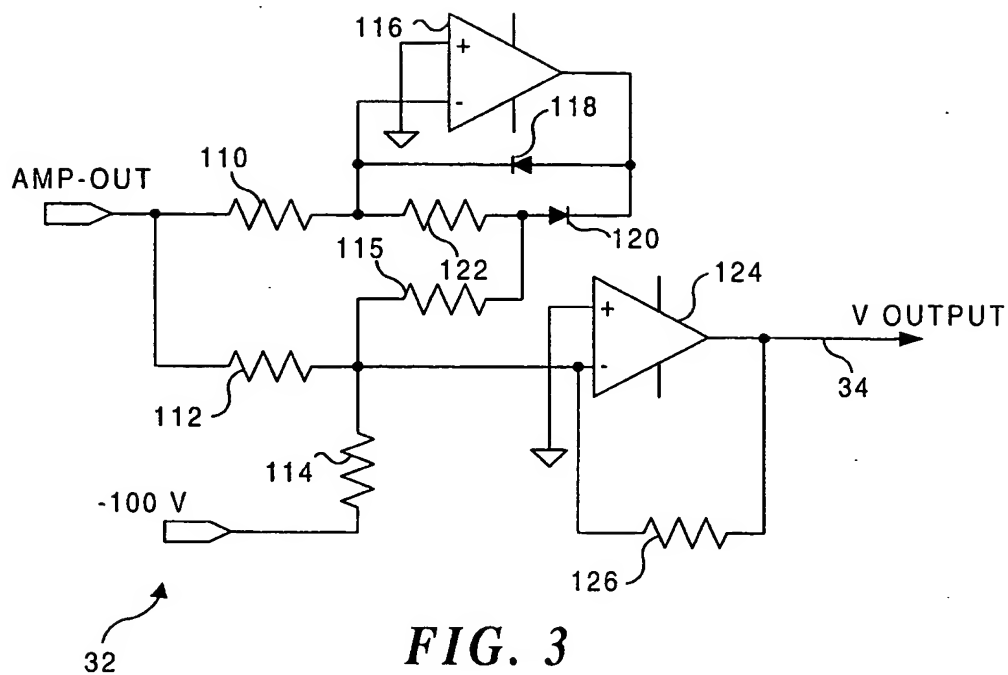
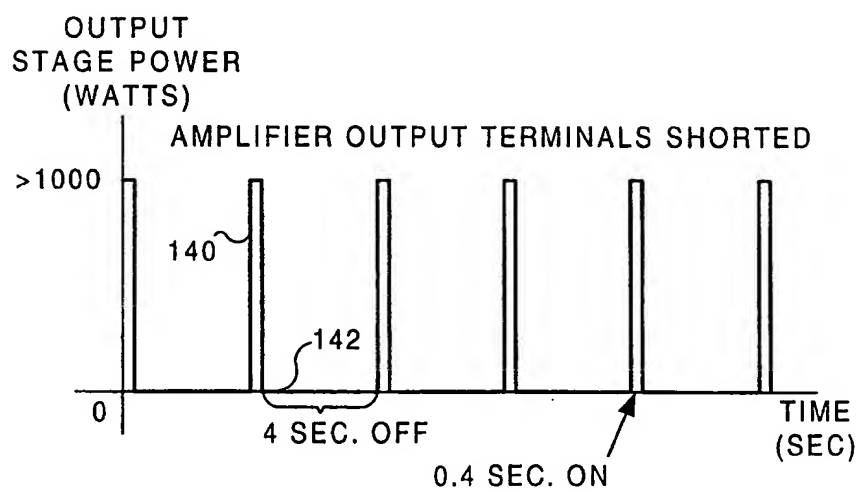


FIG. 1



**FIG. 3****FIG. 4**

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US99/18902

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H02H 3/18

US CL : 361/79; 330/207P

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 361/79, 103; 330/207P, 298, 51

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
NONE

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,458,284 A (OTALA) 03 JULY 1984 (03/07/84), see entire document, especially co. 2, lines 20-41, and col. 3, lines 9-46.	1-3,6,8-11, 15-17,20
Y	US 5,383,083 A (SHINODA et al.) 17 January 1995 (17/01/95), see entire document, especially col. 4, lines 30-46.	1-3,6,8-11, 15-17,20
Y/A	US 4,688,002 A (WINGATE) 18 August 1987 (18/8/87), see entire document, especially col. 4, lines 19-67	1-3,6,8-11, 15-17,20/4, 5, 7, 12-14, 18, 19, 21

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
*A* document defining the general state of the art which is not considered to be of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
*E* earlier document published on or after the international filing date	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*A* document member of the same patent family
*O* document referring to an oral disclosure, use, exhibition or other means	
*P* document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

04 OCTOBER 1999

Date of mailing of the international search report

20 OCT 1999

Name and mailing address of the ISA/US  
Commissioner of Patents and Trademarks  
Box PCT  
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

MICHAEL J SHERRY

Telephone No. (703) 308-1680